REMARKS

This is a full and timely response to the outstanding final Office action mailed on March 28, 2007. Reconsideration and allowance of the application and all pending claims 3 and 8-12, as amended, are respectfully requested.

Present Status of the Application

Applicants have noted with appreciation that the drawing objection, claim objection and the rejections under 35 U.S.C. 112, first and second paragraphs, in the previous Office action dated November 20, 2006, have been rendered moot in light of the amendments to claims 3 and 8-10 and the cancellations to claims 4-7.

The present Office action has objected to claim 3 under 37 C.F.R. 1.75(a) because although this claim meets the requirement 112/2d, i.e., the metes and bounds are determinable, however, specific changes should be made to correct the deficiency set forth in the Office action. Claim 3 is further rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (hereinafter "AAPA"), and further in view of Yamazaki et al. (U.S. Pat. No. 6,392,628 B1, hereinafter "Yamazaki et al."). Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Yamazaki et al. as applied to claim 3 and further in view of Maekawa et al. (U.S. Pat. No. 5,646,642, hereinafter "Maekawa et al."), whereas claims 9-12 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if overcome the claim objection above even though claims 9-12 are objected to as being dependent upon a rejected base claim.

In response thereto, Applicants have amended claim 3 to patentably distinguish the present invention from the cited references of record, and hereby respectfully traverse the rejections of the claims for the reasons provided hereinafter. Reconsideration and withdrawal of the Examiner's rejections are accordingly solicited.

Discussions of Claim Objection

Claim 3 is objected to for failing to particularly pointing out and distinctly claiming the subject matter which the Applicants regard as their invention or discovery. To be more specific, the Examiner asserts that "one of" in line 12 of Applicants' claim 3 should be deleted because a target signal must have two levels.

To rectify said deficiency, Applicants have amended claims 3 as was instructed by the Examiner, and accordingly it is submitted that the objection to claim 3 should be refuted.

Discussions of Claim Rejections under 35 U.S.C. 103(a)

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, and further in view of Yamazaki et al. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Yamazaki et al. as applied to claim 3 and further in view of Maekawa et al.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited

combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

With respect to Applicants' independent claim 3, as amended, it recites,

"A driving stage for an LCD driving circuit, the driving stage being part of the LCD driving circuit in a cascade fashion, the driving stage comprising:

a clock input terminal, for receiving a clock signal having a first original level and a second original level;

a level shifter, coupling to the clock input terminal, for receiving the clock signal from the clock input terminal, operating at a first target level and a second target level, for amplifying the clock signal to a relay signal having a first relay level and a second relay level;

and

an output buffer, coupling to the level shifter, for receiving the relay signal from the level shifter, operating at the first target level and the second target level, for amplifying the relay signal to a target signal having the first target level and the second target level,

wherein the first original level is higher than the second original level, the first target level is higher than the second target level, the first relay level is higher than

the first original level and lower than the first target level, and the second relay level is lower than the second original level and higher than the second target level, **wherein whole power of the driving stage is provided by only two voltage sources**."(Emphasis added)

In paragraph [0013] of the Applicant's disclosure, it reads "only a driving stage with one level shifter and **two voltage sources VDD and VSS are included in the driving stage of LCD driving circuit** according to clock signal amplifying method and driving stage in the present invention". In addition, as supported in paragraph [0044], "[[I]]n both the first and the second preferred embodiments of the present invention, **only one level shifter and two voltage sources (i.e. VDD and VSS)** are required, which consumes substantially lower number of transistors than that **in conventional scheme, where two level shifters and three voltage sources (i.e. VDD, VSS, and GND) are comprised of the driving stage of LCD driving circuit.**" In contrast with AAPA, the present invention is characterized in that the voltage sources of the present invention are limited in the number of two, and thus AAPA does not teach, disclose, or suggest all the technical features of the claim at issue.

Furthermore, in column 10, lines 16-20 of Yamazaki et al, it narrates, "[[A]]s such, by arranging a level shifter circuit before and after the shift register circuit, **the present invention reduces the shift register circuit power supply voltage** so that the shift register circuit TFT is not damaged by punch through or hot electrons due to the short channel effect", connoting an implication that the shift register circuit of Yamazaki

et al. in combination of AAPA is only to reduced power supply voltage and is unlikely to be changed for using only two voltage sources.

In light of the foregoing, the combination of AAPA in view of Yamazaki et al fails to establish a prima facie case of obviousness, and thus the rejection of claim 3 should be obviated.

On the other hand, regarding Applicants' claim 8, it recites the following,

"The driving stage as recited in claim 3 further comprising a dynamic register, wherein the dynamic register couples to the clock input terminal, for receiving the clock signal, and **determines whether to provide the clock signal to the level shifter according to a control signal**." (Emphasis added)

To render the rejection as being unpatentable over AAPA and further in view of Yamazaki et al as applied to claim 3 illegitimate, Applicants' respectfully submit that claim 8 should be allowable as it depends on allowable independent claim 3. Besides, it is submitted that the technical feature of "(the dynamic register) determines whether to provide the clock signal to the level shifter **according to a control signal**" is neither taught nor suggested by Maekawa et al. for the following reasons.

With reference to FIG. 1 of Maekawa et al., the detecting transistor mpA of the detecting/offsetting circuit 1A has three terminals, wherein **the first terminal (the gate) of the detecting transistor mpA is supplied with the input clock signal CK1, and the**

second terminal of the detecting transistor mpA is coupled to the third terminal thereof. Since there is no device disposed between the second terminal and the third terminal, the voltages/signals of the second and the third terminals are identical. Based on the above, as **the input clock signal CK1** is received by the first terminal of the detecting transistor mpA, and both the second and the third terminals are supplied with **the offset clock signal**, no control signal, i.e. purportedly referred to as the signal supplied to the gate electrode of TFT mpA, is observed in Maekawa et al, rendering the rejection set forth in page 5, lines 2-3 improper.

Moreover, in column 3, lines 3-8 of Maekawa et al., it reads, "[[P]]referably, **the above-mentioned level converting block includes a pair of input transistors** which receive at their gates two-phase input clocks having opposite phases. **The input clock signal to be supplied to the gate of one input transistor** is also supplied to a source of the other input transistor." Supported by the above recitation and FIG. 1A of Maekawa et al., the second and the third terminals of the detecting transistor mpA are coupled to the input transistor mn1 and simultaneously receive **the offset clock signal**.

Furthermore, the current source Io coupled to the supplied voltage VDD which is a constant voltage and is unable to be employed as the control signal. Accordingly, as no control signal is observed in FIG. 1 of Maekawa et al, the detecting/offsetting circuit 1A is not capable of utilizing the control signal for monitoring the input of the clock signal.

As such, Applicants present that the rejection of Applicants' claim 8 based upon a combination of references should be withdrawn, for the cited combination of references does not disclose, teach, or suggest, either implicitly or explicitly, all

elements/features/steps of the claim at issue, and thus should also be allowed.

Allowable Subject Matter

Claims 9-12 are deemed allowable but are objected to as being dependent upon a rejected base claim.

Responsive thereto, Applicants submit that claims 9-12 stay unchanged from their original allowable forms. Since now claims 9-12 depend on the allowable base claim 8, they should be allowed as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 3 and 8-12 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,

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